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=> dis his

     (FILE 'USPAT' ENTERED AT 08:53:08 ON 31 AUG 1998)
               ACT C808017/L
               ---------
L1  (      2634)SEA FILE=USPAT (SUBSET OR PARTIAL?) (2A) TRANSFER?
L2  (      9262)SEA FILE=USPAT DMA
L3  (   1458342)SEA FILE=USPAT ADVANTAG? OR BENEFIT#
L4  (         5)SEA FILE=USPAT L1 (P) L2
L5  (         4)SEA FILE=USPAT L3 AND L4
L6  (         1)SEA FILE=USPAT (SUBSET OR PARTIAL?) (3A) DMA TRANSFER?
L7  (         1)SEA FILE=USPAT 5517325/UREF
L8  (         1)SEA FILE=USPAT 5297242/PN
L9  (         1)SEA FILE=USPAT 4635191/PN
L10 (      2642)SEA FILE=USPAT DMA CONTROLLER#
L11 (        46)SEA FILE=USPAT (DMA CONTROLLER#/TI)
L12 (      1889)SEA FILE=USPAT BUS? (2A) RELEAS?
L13 (         8)SEA FILE=USPAT L11 AND L12
L14 (    258604)SEA FILE=USPAT COUNTER#
L15 (     52240)SEA FILE=USPAT RESUM?
L16 (         4)SEA FILE=USPAT L13 AND L15
L17 (         4)SEA FILE=USPAT L14 AND L16
L18 (         1)SEA FILE=USPAT 5517325/UREF
L19 (      1793)SEA FILE=USPAT FIRST PREDETERMINED NUMBER
L20 (         0)SEA FILE=USPAT L11 AND L19
L21 (        22)SEA FILE=USPAT L10 AND L19
L22 (    566396)SEA FILE=USPAT TRANSFER?
L23 (        10)SEA FILE=USPAT L22 (2A) L19
L24 (         0)SEA FILE=USPAT L23 AND L10
              ---------

     FILE 'EPOABS' ENTERED AT 08:53:48 ON 31 AUG 1998
L25          153 S L10
L26           92 S L12
L27           29 S L11
L28            1 S L13
L29         2165 S L15
L30            0 S L16
L31            0 S L17
L32            0 S L18
L33           77 S L19
L34            0 S L20
L35            1 S L21
L36        84405 S L22
L37            0 S L23
L38            0 S L24
L39          142 S L1
L40          484 S L2
L41            0 S L6

     FILE 'JPOABS' ENTERED AT 08:55:55 ON 31 AUG 1998
L42         1067 S L25
L43          467 S L26
L44          184 S L27
L45            4 S L28
L46         2771 S L29
L47            0 S L30
```

L48	0	S	L31
L49	0	S	L32
L50	8	S	L33
L51	0	S	L34
L52	0	S	L35
L53	229646	S	L36
L54	0	S	L37
L55	0	S	L38
L56	260	S	L39
L57	3427	S	L40
L58	1	S	L41

=> dis hit

08-115291

L58: 1 of 1

ABSTRACT:

PURPOSE: To effectively prevent the double access to a data memory without software being conscious of it in the digital signal processor which executes the DMA transfer and processing in parallel according to its own program.

CONSTITUTION: An overhead preventive circuit is provided in the digital signal processor which executes the operation processing between a partial data RAM out of plural data RAMs and another data RAM in parallel with execution of **DMA transfer** between the **partial** data RAM and the outside by the program stored in a program memory. The overhead preventive circuit detects the double access to the data RAM, which is in the middle of DMA execution, in the execution process of the program based on flags SEL0 to SEL3, which indicate that plural data RAMs are in the middle of DMA execution respectively, to stop counting of the program counter, thereby holding the execution of the program.

?show files
File 347:JAPIO Oct 1976-1998/Jan.(UPDATED 980429)
(c) 1998 JPO & JAPIO
File 351:DERWENT WPI 1963-1998/UD=9817;UP=9814;UM=9812
(c)1998 Derwent Info Ltd
?ds

Set	Items	Description
S1	93134	BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BUSING
S2	13013	S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3	248031	(DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSMIS? OR SENT OR SEND? OR ROUT?)
S4	253985	(PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRIBED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5	941	S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FREEING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD?)
S6	183	(PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN?)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7	18	S5 AND (S4 OR S6)(S)S3
S8	9	S7 AND S2

?t8/9/all

8/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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Instant Application

05682930
METHOD FOR TRANSFERRING DATA THROUGH **BUS** AND **BUS MASTER CONTROLLER**

PUB. NO.: 09-297730 [JP 9297730 A]
PUBLISHED: November 18, 1997 (19971118)
INVENTOR(s): HASHIMOTO YUICHI
KAKIAGE TORU
SUZUKI MASATO
KASUGA YOSHIAKI
YASUI JUNICHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-048307 [JP 9748307]
FILED: March 03, 1997 (19970303)
INTL CLASS: [6] G06F-013/362
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the efficiency of data transfer by **releasing** a **bus** corresponding to the presence/absence of request from a 2nd device after the completion of data transfer of a 1st device.

SOLUTION: Based on an output 108 of a counter 4, an output 109 of a counter 5 and an output 111 of an intermittent transfer time register 3, a DMA transfer control part 8 discriminates whether the **prescribed number** of **data** have been completely **transferred** in intermittent transfer or not. When it is discriminated that the **prescribed number** of **data** have been completely **transferred** in the intermittent transfer, the DMA transfer control part 8 finishes the assert of a DMA transfer request signal 104 outputted to a **bus controller** and instructs the **release** of the **bus** . When it is discriminated that all the **data transfers** are completed the DMA transfer control part 8 finishes the assert of the DMA transfer request signal 104 outputted to the **bus controller** 109 and instructs the **release** of the **bus** .

8/9/2 (Item 2 from file: 347)

DIALOG(R)File 347:JAPIO

04956392
IMAGE DATA TRANSFER CONTROLLER

PUB. NO.: 07-248992 [JP 7248992 A]
PUBLISHED: September 26, 1995 (19950926)
INVENTOR(s): SHIMATANI AKIRA
APPLICANT(s): MITA IND CO LTD [000615] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-039562 [JP 9439562]
FILED: March 10, 1994 (19940310)
INTL CLASS: [6] G06F-013/28; G06F-013/362
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 44.7 (COMMUNICATION -- Facsimile)

ABSTRACT

PURPOSE: To provide an image data transfer controller which can perform the effective DMA transfer of image data in accordance with requested conditions for the use of bus.

CONSTITUTION: An image **data transfer** controller is provided with a DMA transfer processing means 7 which repeats the transfer processing to transfer in DMA the image data equivalent to the continuous transfer frequency set after acquisition of the **bus control** right and the **bus** release processing to **release** the acquired **bus control** right in a set **bus releasing** period until a **prescribed number** of image **data** are **transferred** , and a set value changing means 1 which monitors the bus using request state and changes the set continuous transfer frequency and the set bus relasing period based on requested condition for the use of bus.

8/9/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03997661
BUS CONFIGURATION SYSTEM

PUB. NO.: 04-362761 [JP 4362761 A]
PUBLISHED: December 15, 1992 (19921215)
INVENTOR(s): FUKUSHIMA TOMOYOSHI
KANAZAWA NOBUHARU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-138075 [JP 91138075]
FILED: June 11, 1991 (19910611)
INTL CLASS: [5] G06F-013/36
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1534, Vol. 17, No. 239, Pg. 41, May 13, 1993 (19930513)

ABSTRACT

PURPOSE: To improve information transfer efficiency to the utmost even when the number of connected device is increased and a common bus becomes large regarding a bus configuration system in an information processing system connecting plural devices by the common bus.

CONSTITUTION: A bus extension means 300 performing cascade connection of plural common buses 200 connecting devices 100 of less than a **prescribed number** , respectively is provided. The bus extension means is constituted by combining two units of **bus** extension **control** circuit, for instance. When the means receives the **information transmitted** from a device connected with one common bus for which the cascade connection is performed to a device connected with the other common bus, the means is constituted

so that it may **transfer** the receiving **information** to the other common bus, return a response signal for the receiving information to one of the common **bus** and **release** one of the common bus.

8/9/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02718255
DATA **BUS** **CONTROL** SYSTEM

PUB. NO.: 01-015855 [JP 1015855 A]
PUBLISHED: January 19, 1989 (19890119)
INVENTOR(s): KIMURA OSAMU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-171950 [JP 87171950]
FILED: July 09, 1987 (19870709)
INTL CLASS: [4] G06F-013/26
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 867, Vol. 13, No. 191, Pg. 7, May 09, 1989 (19890509)

ABSTRACT

PURPOSE: To optimize the occupied time of a data bus and to smoothly process data by controlling the occupation and the **release** of the data **bus** via a **control** part in response to the quantity of the stored FIFO buffer data and the quantity of the transferred remaining data of a data **bus** **control** system.

CONSTITUTION: A control part 4 of a data **bus** **control** system stores the input data into an FIFO buffer 1 and acquires the occupying right of a data bus 3 to a host device 2b to **transfer** **data** to the bus 3 from the buffer 1. Then the part 4 controls the occupation and the **release** of the **bus** 3 in response to the quantity of the acquired data and the quantity of the **transferred** remaining **data** of the buffer 1. Then a host I/F control part 40, an MPU 43, a **data** **transfer** control part 41, a ROM 44, a RAM 45, etc., are set to the part 4. The bus 3 is occupied when the quantity of data stored in the buffer 1 reaches a **prescribed** **level** and then released when the time needed for reading the quantity of the **transferred** remaining **data** exceeds a **fixed** **level** in an idle state of the buffer 1. Thus the occupied time of the bus 3 is optimized.

8/9/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02245259
CONTROL METHOD FOR **MASTERLESS** SERIAL **BUS** OCCUPATION

PUB. NO.: 62-162159 [JP 62162159 A]
PUBLISHED: July 18, 1987 (19870718)
INVENTOR(s): YAMAOKA HIROMASA
WAKITA AKIHIRO
SAITOU SUMIHISA
AMAHI YASUHIRO
SHIMOYAMA KAZUHIKO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI ENG CO LTD [323361] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-003434 [JP 863434]
FILED: January 13, 1986 (19860113)
INTL CLASS: [4] G06F-013/20; G06F-013/38

JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 651, Vol. 11, No. 399, Pg. 79, December 26, 1987 (19871226)

ABSTRACT

PURPOSE: To attain the control of the occupation of a serial **bus free** from collision of data on a bus by obtaining an optimum transmission queuing time from a transmission PC number in a transmission data format, a transmission time interval set by a setting device, and the amount of transmission data in the transmission data format to set it in the counting devices of the respective PCs.

CONSTITUTION: An MPU 24 reads the self-PC number, the transmission interval, and the total PC **number set** in the setting device 27, and stores them in a memory 26. Then the MPU 24 sets the maximum queuing time in a counting device 25 and comes to a bus monitoring state in order to confirm that there is another PC on the serial bus currently being transmitted. In case there is no PC to be **data -transmitted** on the serial bus, the device 25 supplies to the MPU 24 a transmission timing after the lapsing of the maximum queuing time, and the MPU 24 executes the transmission. After ending the transmission, the MPU 24 gets again the maximum queuing time in the device 25, and executes the arithmetic and control operation. The above described operation is repeated thereafter.

8/9/6 (Item 1 from file: 351)

011167200 **Image available**
WPI Acc No: 97-145125/199713
Related WPI Acc No: 95-240324; 97-077139; 97-414927
XRPX Acc No: N97-120150

Synchronous bus controller **for information processor - has master module transferring address or data to slave module destination via bus and verifying success according to slave acknowledge report**

Patent Assignee: HITACHI LTD (HITA)
Inventor: GEMMA H; KANEKO S; KOMORI K; KONDO N; OKADA T; OKAZAWA K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5604874	A	19970218	US 9360055	A	19930513	D	199713 B
			US 95480395	A	19950607		

Priority Applications (No Type Date): JP 92123569 A 19920515
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5604874	A		24	Div ex	US 9360055	
				Div ex		US 5428753

Abstract (Basic): US 5604874 A

The synchronous **bus controller** has a **bus** , connected to numerous modules. An acknowledge bus line separate from the bus but connected to the modules is used to transmit an acknowledge report. A master module which has acquired **bus mastership control** of a sequence in which the master module executes a transfer cycle for transferring either of an address or data to a slave module of a transfer destination. The master module **releases** the **bus mastership** after the transfer cycle and before a transference of the acknowledge report for the transfer cycle from the slave module.

The slave module which had received either of the **transferred** address or **data** as the slave, controls a sequence in which the slave module sends the acknowledge bus line an acknowledge report indicating receipt of either of the address or the data, a **set number** of cycles after the transfer cycle. The master module which had executed a transfer cycle as the master, then controls a sequence in which the master module verifies success of the transfer in the transfer cycle having been executed, depending on whether the acknowledge report has been received the **set number** of cycles after the transfer cycle.

ADVANTAGE - Enhances bus utilisation factor by reducing overhead of data transfer.
Dwg.2/16
Title Terms: SYNCHRONOUS; BUS; CONTROL; INFORMATION; PROCESSOR; MASTER; MODULE; TRANSFER; ADDRESS; DATA; SLAVE; MODULE; DESTINATION; BUS; VERIFICATION; SUCCESS; ACCORD; SLAVE; ACKNOWLEDGE; REPORT
Derwent Class: T01
International Patent Class (Main): G06F-015/16
File Segment: EPI
Manual Codes (EPI/S-X): T01-G05B; T01-H07A2

8/9/7 (Item 2 from file: 351)
DIALOG(R)File 351:DERWENT WPI

010475570 **Image available**
WPI Acc No: 95-376891/199549
Image data transmission **control device for image forming device e.g. facsimile - has set point change unit to** set **point based on** number **of continuous transmission and demand state of** bus release **period change**
Patent Assignee: MITA IND CO LTD (MTAI)
Inventor: SHIMATANI A
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 7248992	A	19950926	JP 9439562	A	19940310	G06F-013/28	199549 B
US 5517325	A	19960514	US 95395873	A	19950228	H04N-001/21	199625

Priority Applications (No Type Date): JP 9439562 A 19940310
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 7248992	A		6			
US 5517325	A		9			

Abstract (Basic): JP 7248992 A
The image data transmission control device has a CPU (1) to monitor a DMA transmission processing part (7) of an image formed device. The DMA processing part processes DMA transmission of multiple image data by acquiring the right of the **bus control** , repeatedly. The DMA processing part stops the data transfer only after receiving the **bus release control** signal from the central processor unit. A set point change unit is provided to set points based on the number of continuous transmission, and to use demand state of **bus** for **bus release** period change.
ADVANTAGE - Performs efficient DMA transfer.
Dwg.2/4
Abstract (Equivalent): US 5517325 A
An image data transfer controller comprising:
setting means for setting the number of data to be continuously transferred and a **bus release** period;
direct memory access transfer processing means for repeatedly performing transfer processing for acquiring a right to **control** a **bus** and performing direct memory access **transfer** of image **data** corresponding to the **set number** of **data** to be continuously **transferred** and **bus release** processing for **releasing** the acquired right to **control** a **bus** during the set **bus release** period until a **predetermined number** of image **data** are **transferred** ; and
set value changing means for monitoring the state of a request to use said bus and changing the **set** value of said **number** of **data** to be continuously **transferred** and the set value of said **bus release** period on the basis of the state of the request to use the bus.
Dwg.1/5
Title Terms: IMAGE; DATA; TRANSMISSION; CONTROL; DEVICE; IMAGE; FORMING; DEVICE; FACSIMILE; SET; POINT; CHANGE; UNIT; SET; POINT; BASED; NUMBER; CONTINUOUS; TRANSMISSION; DEMAND; STATE; BUS; RELEASE; PERIOD; CHANGE
Derwent Class: T01

International Patent Class (Main): G06F-013/28; H04N-001/[illegible]
International Patent Class (Additional): G06F-013/16; G06F-013/362
File Segment: EPI
Manual Codes (EPI/S-X): T01-H05B2; T01-H05B3

8/9/8 (Item 3 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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004603170
WPI Acc No: 86-106514/198616
XRPX Acc No: N86-078300
Multiple bus cycle reforming microprocessor - selectively generates data control signal while each of predetermined number of bus cycles is being run
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: HULETT T V; MOYER W C; SETERING B A; SPAK M E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 4580213	A	19860401					198616 B

Priority Applications (No Type Date): US 82395957 A 19820707
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 4580213	A		12			

Abstract (Basic): US 4580213 A

A device is provided in a control unit for generating a multicycle signal requesting that a selected number of bus cycles be run using a set of **bus** logic **control** signals. A device in a **data** buffer **transfers** the **data** between the bus and one of a **predetermined number** of destinations in the control unit selected via a data control signal. A device in a **bus** cycle rerun **control** unit responsive to the multi-cycle signal forces the **bus control** unit to run, in accordance with the set of **bus** logic **control** signals, each of the selected number of bus cycles in escess of one, excess of one, for generating for each of the selected number of bus cycles in excess of one an incremented access address for output by the address buffer in response to the address buffer enable signal.

The latter device selectively generates the data control signal while each of the predetermined number of bus cycles are being run. Preferably the set of **bus** logic **control** signals are latched in the **bus control** logic to **release** the control unit.

ADVANTAGE - Capable of performing multiple bus cycles without execution of additional instructions. (12pp Dwg.No.2/7

Title Terms: MULTIPLE; BUS; CYCLE; REFORM; MICROPROCESSOR; SELECT; GENERATE ; DATA; CONTROL; SIGNAL; PREDETERMINED; NUMBER; BUS; CYCLE; RUN
Index Terms/Additional Words: NUMERIC
Derwent Class: T01
International Patent Class (Additional): G06F-011/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-F03

8/9/9 (Item 4 from file: 351)
DIALOG(R)File 351:DERWENT WPI
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004242894
WPI Acc No: 85-069772/198512
XRPX Acc No: N85-052156
Image processing system e.g. for facsimile - has computer bus **and communications** control **allowing data transfer when no image data is being received**
Patent Assignee: CANON KK (CANO)
Inventor: ARIMOTO S

Number of Countries: 006 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
DE 3431985	A	19850314	DE 3431985	A	19840830		198512 B
FR 2551282	A	19850301					198514
JP 60051060	A	19850322	JP 83158452	A	19830830		198518
JP 60051075	A	19850322	JP 83158456	A	19830830		198518
JP 60051076	A	19850322	JP 83158454	A	19830830		198518
GB 2148561	A	19850530	GB 8421879	A	19840830		198522
GB 2148561	B	19880420					198816
CA 1249364	A	19890124					198911
US 5008949	A	19910416	US 90527707	A	19900521		199118

Priority Applications (No Type Date): JP 83158456 A 19830830; JP 83158452 A 19830830; JP 83158454 A 19830830
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
DE 3431985	A		44			

Abstract (Basic): DE 3431985 A

The system has a computer bus, an image processor, a data processor, and a release device permitting data to be transferred from the data processor to the bus when the image processor is receiving no image data from the bus. The image processor has a printer to print the image in accordance with appropriate data from the bus.

The image processor also includes a decoder and a parallel/serial converter. The **release** device **releases** the **bus** whenever a given quantity of image data has been sent. ADVANTAGE - Digital image data can be radially exchanged between reader and recorder. Data as well as images can be processed. The time needed for sending image data via a bus is reduced.

0/8

Abstract (Equivalent): GB 2148561 B

An image processing system comprising: computer control means connected to a computer bus line, for **transmitting** control **data** to other circuit blocks through said **bus** line to **control** the other circuit blocks; means for reading an original image to produce image data; means for compressing image data from said reading means and supplying the compressed image data through the bus line; processing means connected to said bus line for processing compressed image data supplied through said bus line and means for enabling supply of the compressed image data through said bus line whenever a **predetermined amount** of image data has been compressed by the compressing means.

Abstract (Equivalent): US 5008949 A

The image processing system has a device connected to a computer bus line, for supplying compressed image data to the computer bus line. The compressed image data transmitted through the computer bus line is stored. An expanding circuit connected to the store without using the computer bus line expands the compressed image data read out from the store into image data.

A printer connected to the expanding circuit without using the computer bus line, reproduces an image in accordance with the image **data** . **Transfer** of the compressed image data through the computer bus line to the memory whenever a **predetermined amount** of compressed image data is expanded.

USE - For facsimile. (16pp

Title Terms: IMAGE; PROCESS; SYSTEM; FACSIMILE; COMPUTER; BUS; COMMUNICATE; CONTROL; ALLOW; DATA; TRANSFER; NO; IMAGE; DATA; RECEIVE
Derwent Class: T01; W02
International Patent Class (Additional): G06F-005/00; G06F-013/20; G06F-015/20; G06K-009/00; H04N-001/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-D; T01-J04; W02-J03
?

```
Set     Items   Description
S1      93134   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
             SING
S2      13013   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3     248031   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
             IS? OR SENT OR SEND? OR ROUT?)
S4     253985   (PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR E-
             STABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRI-
             BED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR -
             NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5        941   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
             EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
             ?)
S6        183   (PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN?)(3N)(-
             NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR -
             RANGE OR LEVEL? ?)
S7         18   S5 AND (S4 OR S6)(S)S3
S8          9   S7 AND S2
S9       1055   IC="G06F-013/362"
S10       748   IC="G06F 13-362"
S11        76   S9-S10 AND S5
S12         5   S11 AND (S4 OR S6)
S13         2   S12 NOT S8
?t13/9/all
```

13/9/1 (Item 1 from file: 347)

05089162
INFORMATION PROCESSOR

PUB. NO.: 08-044662 [JP 8044662 A]
PUBLISHED: February 16, 1996 (19960216)
INVENTOR(s): IHARA FUJIO
APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-193579 [JP 94193579]
FILED: July 26, 1994 (19940726)
INTL CLASS: [6] **G06F-013/362 ; G06F-013/362**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To prevent use efficiency of a bus from being lowered even when there is the bus slave of low-speed processing in a system.

CONSTITUTION: When requesting processing to bus slaves S(sub 1)-S(sub 3), bus masters M(sub 1)-M(sub 3) acquire the bus use right and issue processing request commands to the bus slaves and afterwards, a shared **bus** 1 is **released** . On the other hand, the bus slaves temporarily store the received commands addressed to them in queues, select any one of them and execute prescribed processing. After the end of processing, an answer command to the bus master of the processing request source is prepared, and a bus using request is issued to a bus arbitrating means 2. Concerning the read request commands continued inside the queue, its arrangement inside the queue is changed so that the higher the request **level** is **set** , the faster the command can be processed. Besides, the more the commands are stored in the queue, the higher the request level of the bus slave is set so that the use right of the shared bus 1 can be speedily acquired.

13/9/2 (Item 1 from file: 351)

011631415 **Image available**
WPI Acc No: 98-048543/199805

XRPX Acc No: N98-038814

Data forwarding method for data processor - involves judging releasing **of** bus **by first apparatus according to existence of request from second apparatus, when forwarding of data is finalized**

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 9297730	A	19971118	JP 9748307	A	19970303	G06F-013/362	199805 B

Priority Applications (No Type Date): JP 9645760 A 19960304

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 9297730	A		11			

Abstract (Basic): JP 9297730 A

The method involves forwarding of **predetermined number** of data among several data, when a first apparatus occupies a bus. When the forwarding of data is finalized, the **releasing** of the **bus** by the first apparatus according to existence of request from a second apparatus, is judged.

ADVANTAGE - Shortens queueing time and enables efficient forwarding of data. Improves data forwarding efficiency.

Dwg.1/5

Title Terms: DATA; FORWARDING; METHOD; DATA; PROCESSOR; JUDGEMENT; RELEASE; BUS; FIRST; APPARATUS; ACCORD; EXIST; REQUEST; SECOND; APPARATUS; FORWARDING; DATA

Derwent Class: T01

International Patent Class (Main): **G06F-013/362**

File Segment: EPI

Manual Codes (EPI/S-X): T01-H05B2; T01-H05B3

?

File 348:EUROPEAN PATENTS 1978-1998/Apr W17
(c) 1998 EUROPEAN PATENT OFFICE
?ds

Set	Items	Description
S1	28884	BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BUSING
S2	6743	S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3	40829	(DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSMIS? OR SENT OR SEND? OR ROUT?)
S4	6925	(DATA OR INFORMATION)(3N)(SENDS OR SENDING)
S5	88048	(PREDETERMINED OR PRESET OR SET OR REFERENCE? OR FIXED OR ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S6	4025	PRESCRIB?(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7	717	S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FREEING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD?)
S8	3913	S5-S6(S)S3-S4
S9	20	S8(S)S7
S10	1	S9/TI,AB,CM

?t10/6,k

10/6,K/1
DIALOG(R)File 348:(c) 1998 EUROPEAN PATENT OFFICE. All rts. reserv.

00170627
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
Communication collision detection.
Nachrichtenkollisionserkennung.
Reconnaissance de collisions d'informations.
LANGUAGE (Publication,Procedural,Application): German; German; German
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	836
CLAIMS B	(German)	EPBBF1	1053
CLAIMS B	(French)	EPBBF1	945
SPEC B	(German)	EPBBF1	3171
Total word count - document A			0
Total word count - document B			6005
Total word count - documents A + B			6005

ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348

...CLAIMS nodes (14) interconnected via a data bus (40), each of said nodes being capable of **transmitting data** , characterized in that the data bus (40) and a spatially separate collision detection reference bus...

...of being gated by a binary signal, to the reference bus (44), with the voltage **level** on the **reference** bus (44) being reduced by a presettable value in the conducting state of the transistor...

...comparators (120, 122) connected thereto which provide signals at their outputs depending on the voltage **level** of the **reference bus** (44) for collision-**free** control of communications over the data bus (40).
8. A circuit arrangement as claimed in...
?

```
Set     Items   Description
S1      28884   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
             SING
S2       6743   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3      40829   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
             IS? OR SENT OR SEND? OR ROUT?)
S4       6925   (DATA OR INFORMATION)(3N)(SENDS OR SENDING)
S5      88048   (PREDETERMINED OR PRESET OR SET OR REFERENCE? OR FIXED OR -
             ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED)(3N)(NUMB-
             ER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE
              OR LEVEL? ?)
S6       4025   PRESCRIB?(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERI-
             C? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7        717   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
             EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
             ?)
S8       3913   S5-S6(S)S3-S4
S9         20   S8(S)S7
S10         1   S9/TI,AB,CM
S11        54   IC="G06F-013/362"
S12         7   S8 AND S11
S13         1   S9 AND S11
S14         1   S13 NOT S10
?t14/5,k
```

14/5,K/1

DIALOG(R)File 348:EUROPEAN PATENTS
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00755441
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348

Peripheral component interconnect bus system having latency and shadow timers

PCI-Bussystem mit Schatten- und Latenzzeitgebern

Systeme de bus-PCI avec horloges de latence et de recopie

PATENT ASSIGNEE:
INTERNATIONAL BUSINESS MACHINES CORPORATION, (200123), , Armonk, NY 10504, (US), (applicant designated states: DE;FR;GB)

INVENTOR:
Pedersen, Mark Eric, 331 South Willard, Burlington, Vermont 05401, (US)

LEGAL REPRESENTATIVE:
de Pena, Alain (15151), Compagnie IBM France Departement de Propriete Intellectuelle, F-06610 La Gaude, (FR)

PATENT (CC, No, Kind, Date): EP 710913 A1 960508 (Basic)
APPLICATION (CC, No, Date): EP 95480160 951024;
PRIORITY (CC, No, Date): US 337008 941107
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-013/40; **G06F-013/362**

ABSTRACT EP 710913 A1

A PCI system is provided with a shadow register and a shadow timer. When a master device sends an address designating a target device that is connected to another bus, the device's latency value is recorded in the shadow register. While the PCI-PCI bridge arbitrates for the target bus, the master's latency timer increments but the shadow timer will not begin to increment until the PCI-PCI bridge receives a grant# from the target's bus and data transmission begins. Accordingly, the bus arbiter will not de-assert the grant# until the shadow timer has reached the latency value or the master device has released the bus after completing its data transmission. This ensures that the master device will be allocated a time period equal to its latency value to transmit data.
(see image in original document)
ABSTRACT WORD COUNT: 155

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 960508 A1 Published application (A1with Search Report ;A2without Search Report)

Examination: 961113 A1 Date of filing of request for examination: 960914
Withdrawal: 980114 A1 Date on which the European patent application was withdrawn: 971120
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	885
SPEC A	(English)	EPAB96	3588
Total word count - document A			4473
Total word count - document B			0
Total word count - documents A + B			4473

ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348
...INTERNATIONAL PATENT CLASS: **G06F-013/362**

...SPECIFICATION bus 90, then the I/O-DMA master 110 would have only one cycle to **transfer data** before it would be required to **release** the primary **bus** 80. As a result, peripheral device 100 would be able to **transfer data** during only one cycle instead of the **number** of cycles **defined** by its latency value L1. Accordingly, if this situation occurs, only a small part of...

...device 100 during the time PCI-PCI bridge 70 arbitrates for secondary bus 90. Since **data** was **transmitted** only during one cycle, the wasted period is commensurable with the latency value L1.
Alternatively...
?

```
Set     Items   Description
S1      28884   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
             SING
S2       6743   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3      40829   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
             IS? OR SENT OR SEND? OR ROUT?)
S4       6925   (DATA OR INFORMATION)(3N)(SENDS OR SENDING)
S5      88048   (PREDETERMINED OR PRESET OR SET OR REFERENCE? OR FIXED OR -
             ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED)(3N)(NUMB-
             ER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE
              OR LEVEL? ?)
S6       4025   PRESCRIB?(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERI-
             C? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7        717   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
             EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
             ?)
S8       3913   S5-S6(S)S3-S4
S9         20   S8(S)S7
S10         1   S9/TI,AB,CM
S11        54   IC="G06F-013/362"
S12         7   S8 AND S11
S13         1   S9 AND S11
S14         1   S13 NOT S10
S15       256   S7(S)S3-S4
S16        23   S15/TI,AB
S17         2   S16 AND S11
S18         1   S17 NOT (S10 OR S14)
?t18/5,k
```

18/5,K/1

DIALOG(R)File 348:EUROPEAN PATENTS

00571955
ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348

Arbitratian control between host system and connected subsystem.
Arbitrierungssteuerung zwischen Wirtsystem und verbundenen Untersystemen.
Commande d'arbitrage entre systeme hote et sous-systeme connecte.

PATENT ASSIGNEE:
INTERNATIONAL BUSINESS MACHINES CORPORATION, (200125), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Drerup, Bernard Charles, 8543 Capitol of Texas Highway No. 3085, Austin, Texas 78759, (US)
Peterson, James Chester, 8800 Crest Ridge Circle, Austin, Texas 78750, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 564116 A1 931006 (Basic)
APPLICATION (CC, No, Date): EP 93301923 930312;
PRIORITY (CC, No, Date): US 857880 920326
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-013/40; **G06F-013/362**
CITED PATENTS (EP A): US 4868741 A; US 4868741 A; EP 518504 A; EP 518504 A; US 4257099 A; GB 2131581 A

ABSTRACT EP 564116 A1

A method and apparatus are disclosed for allowing at least one computer subsystem (61), having a central arbiter (63), to be interconnected with a host system (51) also including a central arbiter (53). Conversion logic (100) is added to each computer subsystem desired to be interconnected to the host. The conversion logic is positioned between the arbitration buses of the host system and the subsystem and includes two requesting arbiters, one of which arbitrates for the host system arbitration bus, and the other which arbitrates for the subsystem arbitration bus. At the default state, the conversion logic has successfully arbitrated for, and is maintaining control of the subsystem

. bus. After a request from a subsystem device for access to the host bus, the conversion logic arbitrates for control of the host bus. When control of the host bus is awarded to the conversion logic, control of the subsystem **bus** is **released** and the requesting subsystem device can **transfer** **data** between the subsystem and host. (see image in original document)

ABSTRACT WORD COUNT: 171

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	931006 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	940302 A1	Date of filing of request for examination: 931227
*Assignee:	970205 A1	Applicant (transfer of rights) (change): International Business Machines Corporation (200120) Old Orchard Road Armonk, N.Y. 10504 (US) (applicant designated states: DE;FR;GB)
Withdrawal:	970409 A1	Date on which the European patent application was withdrawn: 970130

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	820
SPEC A	(English)	EPABF1	6364
Total word count - document A			7184
Total word count - document B			0
Total word count - documents A + B			7184

ORDER fax of complete patent from Dialog SourceOne. See HELP ORDER 348

...INTERNATIONAL PATENT CLASS: **G06F-013/362**

...ABSTRACT control of the host bus is awarded to the conversion logic, control of the subsystem **bus** is **released** and the requesting subsystem device can **transfer** **data** between the subsystem and host. (see image in original document)

?

File 16:IAC PROMT(R) 1972-1998/May 01
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File 88:IAC BUSINESS A.R.T.S. 1976-1998/May 01
(c) 1998 Information Access Co.
File 148:IAC Trade & Industry Database 1976-1998/May 01
(c) 1998 Info Access Co
File 275:IAC(SM) Computer Database(TM) 1983-1998/May 01
(c) 1998 Info Access Co
File 570:IAC MARS(R) 1984-1998/May 01
(c) 1998 Information Access Co.
File 621:IAC New Prod.Annou.(R) 1985-1998/May 01
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(c) 1998 McGraw-Hill Co. Inc
File 636:IAC Newsletter DB(TM) 1987-1998/May 01
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File 647:CMP Computer Fulltext 1988-1998/Mar W5
(c) 1998 CMP
File 674:Computer News Fulltext 1989-1998/Apr W4
(c) 1998 IDG Communications
?ds

Set	Items	Description
S1	2799055	BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BUSING
S2	20955	S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3	341619	(DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSMIS? OR SENT OR SEND? OR ROUT?)
S4	154433	(PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRIBED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5	3263	S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FREEING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD?)
S6	260	(PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN? OR PRE()(STIPUL? OR ARRANG? OR DECID? OR ORDAIN?))(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7	10	S5(S)(S4 OR S6)
S8	10	RD S7 (unique items)

?t8/3,k/all

8/3,K/1 (Item 1 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
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05093025 SUPPLIER NUMBER: 09858899 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Canada sets new farm income safety net programs.
Milling & Baking News, v69, n48, p29(1)
Jan 29, 1991
ISSN: 0091-4843 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1070 LINE COUNT: 00083

... worked out, the government indicated that a Saskatchewan wheat farmer with an average long-term **yield** of 30 **bus** an acre would be guaranteed C$120 an acre for No. 2 Canadian western red...

...uncertainty prevailed over whether the figure of C$4 a bu would be the eventual **target level** , or whether it was used merely as an example, but Harvey McEwen, president of the...

8/3,K/2 (Item 1 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1998 Info Access Co. All rts. reserv.

01607866 SUPPLIER NUMBER: 14011457 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Networking: wireless datacom sparks mobile revolution. (OEM Integration supplement: perspectives on OEM integration)
Caruthers, Frank
Computer Design, v32, n5, pS11(7)
May, 1993
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5259 LINE COUNT: 00420

... messages from any of several different wireless connections. The stack cache architecture also reduces the **number** of external data **references** . Since the processor accesses the bus less often, it consumes less power and **frees** **bus** bandwidth for communications traffic.
Despite its performance--AT&T has released benchmarks in which the...

8/3,K/3 (Item 2 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
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01121781 SUPPLIER NUMBER: 00660440
SCSI Takes on Additional I-O Tasks.
Williams, T.
Computer Design, v24, n12, p33-34
Sept. 15, 1985
DOCUMENT TYPE: evaluaton ISSN: 0010-4566 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

...ABSTRACT: host computer and intelligent peripherals and it provides for vendor-unique commands and a well-**defined** **set** of high-**level** commands, which are needed to access all the features of optical disk drives. To become...

...and tape market. A method to allow SCSI devices will have to be able to **relinquish** the **bus** when they are not actually transferring data, and then reestablish the connection 'thread' without any...

8/3,K/4 (Item 1 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00509031 00509031

First Scientific Frame Grabber on PCI Bus Announced by Data Translation

News Release
DATELINE: MARLBORO, MA February 6, 1995 WORD COUNT: 1060

...Master, image data
transfers to the CPU quickly, thus decreasing overall processing time.
The PC! **bus** **frees** imaging applications from the severe built-in bandwidth limitations of 15A or E!SA, which...

...to
installed PnP- compliant boards on the system itself. The user no longer needs to **set** base address, interrvpt **levels** or any other configuration element at installation or later. Instead, a PnP board tells the...

8/3,K/5 (Item 2 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)
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00326704 00326704

Open-architecture local bus scheme cuts costs for industrial computer

system builders

News Release
DATELINE: Cambridge, United Kingdom April 30, 1992 WORD COUNT: 770

...cuts costs for industrial computer
system builders
- runs on STE, VME and PCbus
Arcom has **released** a new mezzanine **bus** scheme offering powerful and cost-effective local expansion facilities for industrial computer system builders. It combines rvggedness with a wide range of signals, overcoming major shortcomings of previous local **buses** . It is **released** with an extensive choice of ready-to-use modules for VMEbus, STEbus and PCbus host...

...real-time systems applications: more interrupts, DMA
channels, and three serial lines - the latter being **targetted** towards the growing **number** of industrial ICs offered with serial control mechanisms like I2C or Microwire (for example, ADCs...

8/3,K/6 (Item 3 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)

00279235 00279235

MOTOROLA SHIPPING 68040 IN VOLUME

PR Newswire
DATELINE: AUSTIN, TX November 26, 1990 WORD COUNT: 968

...memory. As a result,
main memory needs to be updated less frequently, leaving the system **bus free** to perform other functions on demand.
Full Compatibility
Although it embodies a complete redesign of...

...End Microprocessor Division, the Microcontroller Division and the Digital Signal Processor Operation. The Group has **established** a **number** of industry-standard architectures, including the 68000 and 88000 families of microprocessors, the 68HC05, 68HC11...

8/3,K/7 (Item 4 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)

00268871 00268871

New Interface Kit Simplifies GPIB Instrument Control Using SCSI Port of DEC VAXstation 3100 or MicroVAX 3100 Workstations

News Release
DATELINE: Austin, TX July 23, 1990 WORD COUNT: 603

...a 64K RAM buffer for storing data sent from the SCSI port, leaving the SCSI **bus free** to do other tasks while the GPIB-SCSI communicates with a GPIB device.
The GPIB11...

...a device driver that is
installed within the operating system. The driver consists of a **set** of fast, low-**level** and high-level tunctions that control the GPIB-SCSI interface. The handler implements over 25...

8/3,K/8 (Item 5 from file: 621)

DIALOG(R)File 621:IAC New Prod.Annou.(R)

00129854 00129854

QG-1280 & QG-640 High Performance Micro VAX Graphic Controllers

DATELINE: Dorval, Quebec May 30, 1986 WORD COUNT: 408

...at full bus speed. The QG-640 and QG-1280 both use the same high **level** graphic instruction **set** . This graphic code compatibility allows for easy porting of an application program from one resolution to another. This high **level** instruction **set** is designed to allow the on board graphic processors do the drawing while **freeing** up the Q-**bus** CPU and allowing it to run the application program.
Pricing on the QG-1280 is...

8/3,K/9 (Item 6 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)

00121066 00121066

INTELLIGENT VMEbus 9-TRACK TAPE CONTROLLER

DATELINE: Campbell, CA January 22, 1986 WORD COUNT: 199

...systems.
THE SVME-176 FRATURES:
support 9-track tape drives with standard Pertec interface high-**level** command **set** for software interface in firmware included power-up controller diagnostics data scatter/gather commands supports...

...indication local reset by faceplate pushbutton jumper-selectable ROR/RWD VMEbus arbitration jumper-selectable VMEbus **bus** request level early **release** of BBSY to allow for early arbitration.
The SVME-716 lists at $2,100.00...

8/3,K/10 (Item 7 from file: 621)
DIALOG(R)File 621:IAC New Prod.Annou.(R)

00109947 00109947

EMULEX INTRODUCES HOST ADAPTER WHICH CONNECTS PC TO SCSI PERIPHERALS

DATELINE: Costa Mesa, CA October 25, 1985 WORD COUNT: 526

...Small Computer Systems Interface (SCSI) peripherals.
SCSI is an intelligent bus which uses a high-**level** command **set** to mask the internal structures of the peripheral from the interface, making SCSI device-independent...

...disconnect/reconnect. Using
this feature, drives which are performing time-consuming tasks (i.e., seeks) **release** the **bus** temporarily and reconnect when the seek has been completed. Support of this feature permits the...

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File   2:INSPEC 1969-1998/Apr W4
         (c) 1998 Institution of Electrical Engineers
File   6:NTIS 64-1998/May W4
         Comp&distr 1998 NTIS, Intl Copyright All Righ
File   8:Ei Compendex(R) 1970-1998/May W5
         (c) 1998 Engineering Info. Inc.
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         (c) 1998 BLDSC all rts. reserv.
File  77:Conference Papers Index 1973-1998/May
         (c) 1998 Cambridge Sci Abs
File  94:JICST-EPlus 1985-1998/Mar W1
         (c)1998 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-1998/Mar
         (c) 1998 The HW Wilson Co.
File 108:Aerospace Database 1962-1998/Apr
         (c) 1998 AIAA
File 144:Pascal 1973-1998/Apr
         (c) 1998 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-1998/Apr
         (c) 1998 Reed-Elsevier (UK) Ltd.
File 434:Scisearch(R) Cited Ref Sci 1974-1998/Apr W3
         (c) 1998 Inst for Sci Info
?ds

Set     Items   Description
S1      82862   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
             SING
S2       5546   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3     184593   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
             IS? OR SENT OR SEND? OR ROUT?)
S4      99786   (PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR E-
             STABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRI-
             BED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR -
             NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5        370   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
             EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
             ?)
S6         18   (PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN? OR PR-
             E()(STIPUL? OR ARRANG? OR DECID? OR ORDAIN?))(3N)(NUMBER? OR -
             QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LE-
             VEL? ?)
S7          0   S5 AND (S4 OR S6)
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S1	4362	BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BUSING
S2	476	S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3	9043	(DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSMIS? OR SENT OR SEND? OR ROUT?)
S4	998	(PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR ESTABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRIBED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5	88	S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FREEING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD?)
S6	0	(PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN? OR PRE()(STIPUL? OR ARRANG? OR DECID? OR ORDAIN?))(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S7	0	S5 AND (S4 OR S6)

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S1       3086   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
            SING
S2        177   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3      16898   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
            IS? OR SENT OR SEND? OR ROUT?)
S4      10170   (PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR E-
            STABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRI-
            BED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR -
            NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5         18   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
            EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
            ?)
S6          3   (PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN? OR PR-
            E()(STIPUL? OR ARRANG? OR DECID? OR ORDAIN?))(3N)(NUMBER? OR -
            QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LE-
            VEL? ?)
S7          0   S5 AND (S4 OR S6)
?
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Set     Items   Description
S1     101588   BUS OR BUSSES OR BUSSED OR BUSSING OR BUSES OR BUSED OR BU-
             SING
S2       4023   S1(2N)(CONTROL? OR MASTER? OR REGULAT? OR MANAG?)
S3     109929   (DATA OR INFORMATION)(3N)(TRANSFER? OR TRANSMIT? OR TRANSM-
             IS? OR SENT OR SEND? OR ROUT?)
S4      69781   (PREDETERMINED OR PRESET OR SET OR REFERENC? OR FIXED OR E-
             STABLISHED OR PREESTABLISHED OR TARGET? OR DEFINED OR PRESCRI-
             BED OR PREDEFINED)(3N)(NUMBER? OR QUANTITY? OR QUANTITIES OR -
             NUMERIC? OR AMOUNT? OR RANGE OR LEVEL? ?)
S5       1488   S1(3N)(RELEAS? OR RELINQ? OR FREE OR FREES OR FREED OR FRE-
             EING OR DISENGAG? OR UNENGAG? OR (DIS OR UN)()ENGAG? OR YIELD-
             ?)
S6        112   (PRESTIPUL? OR PREARRANG? OR PREDECID? OR PREORDAIN? OR PR-
             E()(STIPUL? OR ARRANG? OR DECID? OR ORDAIN?))(3N)(NUMBER? OR -
             QUANTITY? OR QUANTITIES OR NUMERIC? OR AMOUNT? OR RANGE OR LE-
             VEL? ?)
S7          0   S5(S)(S4 OR S6)
?
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